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Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row P							
1	USB_VDDA33	2	USB_DP	3	mLCD_DB_14	4	mLCD_DB_13
5	mLCD_DB_7	6	mLCD_DB_3	7	mLCD_DB_5	8	mLCD_RS
9	mLCD_DB_1	10	TMS	11	I2SRX_WS0	12	UART_RXD
13	TRST_N	14	mUART_RTS_N	-	-	-	-

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset [2]	Cell type [3]	Description
Clock Generation Unit (CGU)						
FFAST_IN	A10	SUP1	AI	-	AIO2	12 MHz oscillator clock input.
FFAST_OUT	B10	SUP1	AO	-	AIO2	12 MHz oscillator clock output.
VDDA12	D11; E10	SUP1	Supply	-	PS3	12 MHz oscillator/PLLs analog supply.
VSSA12	E9	-	Ground	-	CG1	12 MHz oscillator/PLLs analog ground.
RSTIN_N	H14	SUP3	DI	I:PU	DIO2	System Reset Input (active LOW).
CLK_256FS_O	H12	SUP3	DO	O	DIO1	Programmable clock output; fractionally derived from CLK1024FS_BASE clock domain. Generally used for external audio codec master clock.
CLOCK_OUT	J4	SUP4	DO	O	DIO4	Programmable clock output; fractionally derived from SYS_BASE clock domain.
SYSCLK_O [4]	G13	SUP3	DO	O	DIO1	Programmable clock output. Output one of seven base/reference input clocks. No fractional divider.
10-bit ADC						
ADC10B_VDDA33	A13	SUP3	Supply	-	PS3	10-bit ADC analog supply.
ADC10B_GNDA	A12	-	Ground	-	CG1	10-bit ADC analog ground.
ADC10B_GPA0	B14	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA1	A14	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA2	B13	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA3	C14	SUP3	AI	-	AIO1	10-bit ADC analog input.
USB HS 2.0 OTG						
USB_VBUS	L2	SUP5	AI	-	AIO3	USB supply detection line.
USB_ID	M1	SUP3	AI	-	AIO1	Indicates to the USB transceiver whether in device (USB_ID HIGH) or host (USB_ID LOW) mode (contains internal pull-up resistor).
USB_RREF	J5	SUP3	AIO	-	AIO1	USB connection for external reference resistor (12 kΩ ± 1%) to analog ground supply.
USB_DP	P2	SUP3	AIO	-	AIO1	USB D+ connection with integrated 45 Ω termination resistor.

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Table 4. Pin description *…continued*

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
I²S/digital audio output						
mI2STX_DATA0[4]	M13	SUP3	DO/GPIO	O	DIO1	I²S serial data transmit output.
mI2STX_BCK0[4]	M12	SUP3	DO/GPIO	O	DIO1	I²S bit clock.
mI2STX_WS0[4]	M11	SUP3	DO/GPIO	O	DIO1	I²S word select.
mI2STX_CLK0[4]	N14	SUP3	DO/GPIO	O	DIO1	I²S serial clock.
I2STX_DATA1[4]	F12	SUP3	DO/GPIO	O	DIO1	I²S serial data transmit output.
I2STX_BCK1[4]	E14	SUP3	DO/GPIO	O	DIO1	I²S bit clock.
I2STX_WS1[4]	G10	SUP3	DO/GPIO	O	DIO1	I²S word select.
General Purpose IO (GPIO)						
GPIO0[7]	K10	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 0 (mode pin 0).
GPIO1[7]	J10	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 1 (mode pin 1).
GPIO2[7]	L14	SUP3	GPIO	I	DIO1	General Purpose IO pin 2 (mode pin 2).
GPIO3	B11	SUP3	GPIO	I	DIO1	General Purpose IO pin 3.
GPIO4	C11	SUP3	GPI	I	DIO1	General Purpose input pin 4.
mGPIO5[4]	B6	SUP3	GPIO	I	DIO4	General Purpose IO pin 5.
mGPIO6[4]	A6	SUP3	GPIO	I	DIO4	General Purpose IO pin 6.
mGPIO7[4]	A5	SUP3	GPIO	I	DIO4	General Purpose IO pin 7.
mGPIO8[4]	B5	SUP3	GPIO	I	DIO4	General Purpose IO pin 8.
mGPIO9[4]	C5	SUP3	GPIO	I	DIO4	General Purpose IO pin 9.
mGPIO10[4]	A4	SUP3	GPIO	I	DIO4	General Purpose IO pin 10.
GPIO11	H13	SUP3	GPIO	I	DIO1	General Purpose IO pin 11.
GPIO12	H10	SUP3	GPIO	I	DIO1	General Purpose IO pin 12.
GPIO13	J12	SUP3	GPIO	I	DIO1	General Purpose IO pin 13.
GPIO14	J14	SUP3	GPIO	I	DIO1	General Purpose IO pin 14.
GPIO15	J13	SUP3	GPIO	I	DIO1	General Purpose IO pin 15.
GPIO16	J11	SUP3	GPIO	I	DIO1	General Purpose IO pin 16.
GPIO17	K12	SUP3	GPIO	I	DIO1	General Purpose IO pin 17.
GPIO18	K14	SUP3	GPIO	I	DIO1	General Purpose IO pin 18.
GPIO19	H11	SUP3	GPIO	I	DIO1	General Purpose IO pin 19.
GPIO20	K13	SUP3	GPIO	I	DIO1	General Purpose IO pin 20.
External Bus Interface (EBI)/NAND flash controller						
EBI_A_0_ALE[4]	B3	SUP4	DO	O	DIO4	EBI address latch enable.
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI command latch enable.
EBI_D_0[4]	G2	SUP4	DIO	I	DIO4	EBI data I/O 0.
EBI_D_1[4]	F2	SUP4	DIO	I	DIO4	EBI data I/O 1.
EBI_D_2[4]	F1	SUP4	DIO	I	DIO4	EBI data I/O 2.
EBI_D_3[4]	E1	SUP4	DIO	I	DIO4	EBI data I/O 3.
EBI_D_4[4]	E2	SUP4	DIO	I	DIO4	EBI data I/O 4.

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10. Application information

Table 28. LCD panel connections

TFBGA pin #	Pin name	Reset function (default)	LCD mode					
			Parallel					Serial
			LCD panel data mapping			Control function		
			16 bit	8 bit	4 bit	6800	8080	
K8	mLCD_CSB/EBI_NSTCS_0	LCD_CSB	-	-	-	LCD_CSB	LCD_CSB	LCD_CSB
L8	mLCD_E_RD/EBI_CKE	LCD_E_RD	-	-	-	LCD_E	LCD_RD	-
P8	mLCD_RS/EBI_NDYCS	LCD_RS	-	-	-	LCD_RS	LCD_RS	LCD_RS
N9	mLCD_RW_WR/EBI_DQM_1	LCD_RW_WR	-	-	-	LCD_RW	LCD_WR	-
N8	mLCD_DB_0/EBI_CLKOUT	LCD_DB_0	LCD_DB_0	-	-	-	-	-
P9	mLCD_DB_1/EBI_NSTCS_1	LCD_DB_1	LCD_DB_1	-	-	-	-	-
N6	mLCD_DB_2/EBI_A_2	LCD_DB_2	LCD_DB_2	-	-	-	-	-
P6	mLCD_DB_3/EBI_A_3	LCD_DB_3	LCD_DB_3	-	-	-	-	-
N7	mLCD_DB_4/EBI_A_4	LCD_DB_4	LCD_DB_4	-	-	-	-	-
P7	mLCD_DB_5/EBI_A_5	LCD_DB_5	LCD_DB_5	-	-	-	-	-
K6	mLCD_DB_6/EBI_A_6	LCD_DB_6	LCD_DB_6	-	-	-	-	-
P5	mLCD_DB_7/EBI_A_7	LCD_DB_7	LCD_DB_7	-	-	-	-	-
N5	mLCD_DB_8/EBI_A_8	LCD_DB_8	LCD_DB_8	LCD_DB_0	-	-	-	-
L5	mLCD_DB_9/EBI_A_9	LCD_DB_9	LCD_DB_9	LCD_DB_1	-	-	-	-
K7	mLCD_DB_10/EBI_A_10	LCD_DB_10	LCD_DB_10	LCD_DB_2	-	-	-	-
N4	mLCD_DB_11/EBI_A_11	LCD_DB_11	LCD_DB_11	LCD_DB_3	-	-	-	-
K5	mLCD_DB_12/EBI_A_12	LCD_DB_12	LCD_DB_12	LCD_DB_4	LCD_DB_0	-	-	-
P4	mLCD_DB_13/EBI_A_13	LCD_DB_13	LCD_DB_13	LCD_DB_5	LCD_DB_1	-	-	SER_CLK
P3	mLCD_DB_14/EBI_A_14	LCD_DB_14	LCD_DB_14	LCD_DB_6	LCD_DB_2	-	-	SER_DAT_IN
N3	mLCD_DB_15/EBI_A_15	LCD_DB_15	LCD_DB_15	LCD_DB_7	LCD_DB_3	-	-	SER_DAT_OUT

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